The Easy Way to Achieve ECO Success Easylogic

Performing Scan Chain Fixing during Functional ECO Process

ScanChainECO Application note
App-DFT-01

ScanChainECO offers three major features in DFT to its users:

1. Automatic scan chain stitching
2. Automatic balancing of scan chain length
3. Manual stitching for greater flexibility in adhering to DFT design rules

ScanChainECO significantly shortens the time required for each functional ECO task. This application note provides a brief introduction to how ScanChainECO manages the addition and removal of Scan DFFs.

Overview

After a functional change, designers typically need to perform scan chain stitching or removal if there are added or deleted FFs in the design netlist. Manual work is manageable if the number of added or deleted FFs is small. However, as the number of affected FFs increases, designers must invest significant amount of time tracing relevant scan chain information such as scan clock source, each chain length, scan-related functionality, and compressor circuits. Fixing the scan chain is not only non-productive work but also a complex task that easily surpasses human capabilities, causing designers to compromise on the DFT coverage of these affected FFs or even abandon the ECO entirely.

For designers seeking solutions to fix scan chains, Easylogic’s solution proves invaluable.

Major Features of ScanChainECO

ScanChainECO can produce excellent results in the following four areas:

- Automatic scan chain stitching
- Automatic scan chain balancing
- Optional manual stitching function
- Manual removal of test registers connected to the scan chain

Details for these functions are explained below.

(1) Automatic Scan Chain Stitching

The automatic scan chain stitching function accelerates scan chain ECO completion, minimizing the risk of human errors inherent in manual scan chain handling, thus ensuring efficiency and accuracy.

ScanChainECO first separates the DFT function from the logic function based on the Disable DFT constraints provided by the user. Subsequently, it tracks the relevant scan chains based on the compressor tail input pins declared by the user. If there is an SDFF that needs to be removed, the SDFF/Q and SDFF/SI of this SDFF will be tied together. Conversely, if there is a new DFF that needs to be added to the chain, ScanChainECO will automatically insert it in a suitable location based on parent module's conditions, such as clock source and chain length of the new DFF, to ensure the result meets the DRC requirements for DFT.

In the example below (Figure 1), if Inst:X and Inst:Z are connected to the compressor circuit, and the clock source of the newly added DFF in the ECO is CLKA_1, located inside module B, ScanChainECO will connect the new DFF to either net P0 or net P1. If P0 is closer to the middle point of the entire chain, eco_T will be connected to P0; otherwise, it will be connected to P1.

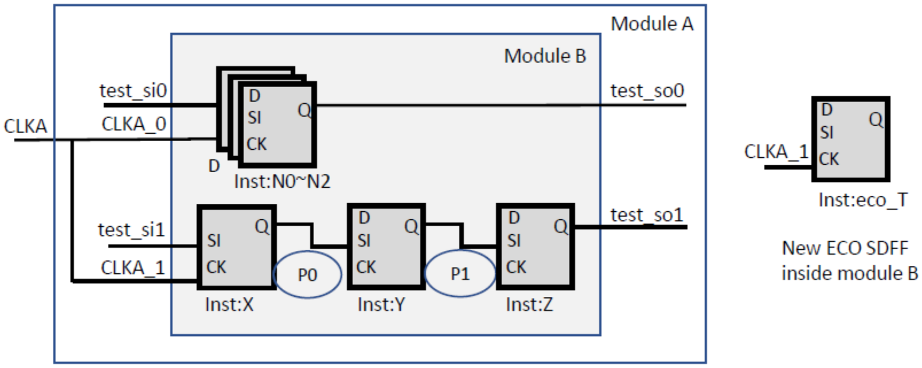


Figure 1: Automatically connecting the new ECO SDFF to net P0 or net P1

(2) Automatic chain length balancing

In addition to reducing ECO turnaround time, automatic scan chain balancing ensures that chip testing cost is not increased due to the ECO.

ScanChainECO automatically tracks the length of all scan chains based on user's DFT settings. It inserts the new ECO DFF into the existing chain, ensuring that the length of the scan chain stays within the required range.

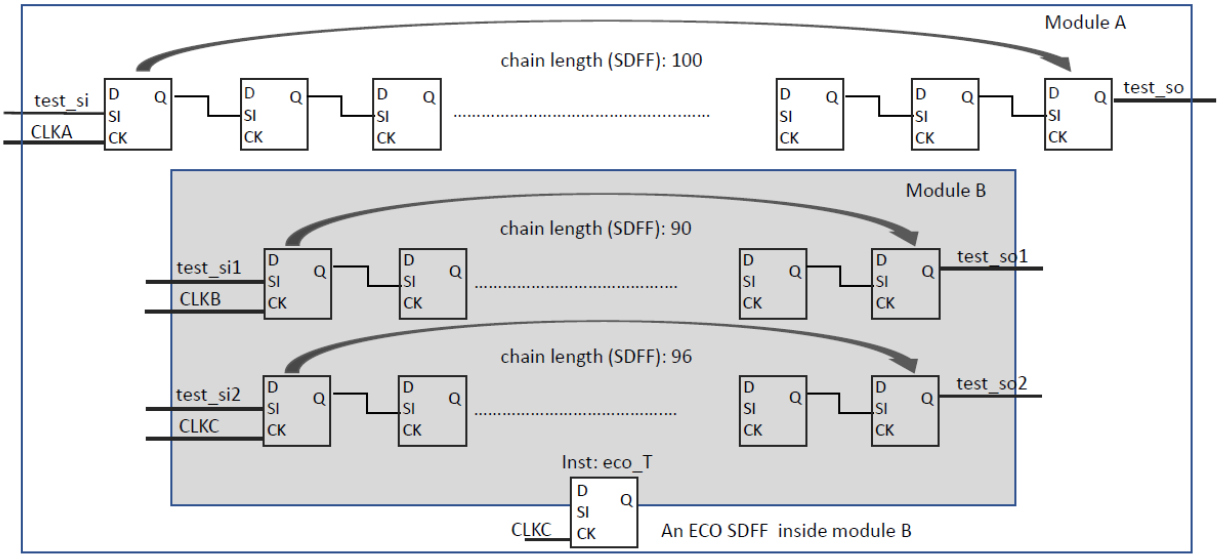


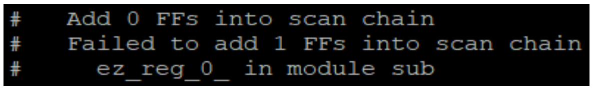
Figure 2: Automatic chain length balancing

Users can use the following constraint to limit the length of all scan chains, which also helps in balancing.

```
set_max_chain_length
```

In the example (Figure 2), assuming the longest chain length is 100, and the clock source of the newly added ECO DFF is CLKC and it is inside module B, eco_T will be inserted to the middle point between test_si2 and test_so2, which is the 49th position.

If any condition required to stitch the scan chain cannot be fulfilled, such as the requirements for max chain length or the need for the same clock source, it will result in failure, with the corresponding message provided in the log file. Here is an example (Figure 3).



```
#    Add 0 FFs into scan chain
#    Failed to add 1 FFs into scan chain
#      ez_reg_0_ in module sub
```

Figure 3: Failure message of chain length balancing

(3) Manual Stitching

Manual stitching is an additional feature that gives users greater freedom in complying with their DFT design rules. Users can declare the connection of chain members within the ScanChainECO environment precisely. This feature is useful in the following scenarios:

a. ScanChainECO cannot complete the required scan chain stitching, or
b. Timing issues, or
c. P&R congestion issues.

In the example below (Figure 4), the original scan chain sequence is:

xxx/Q → b_reg3 → yyy/SI

After determining an appropriate SDFF location (such as b_reg3), users can connect the new SDFF to that location directly, and declare the connection of the chain members, using the following commands.

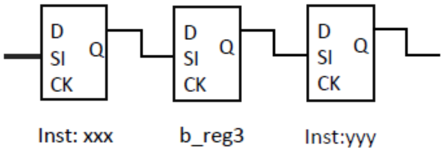


Figure 4: Original scan chain sequence

```
insert_reg_into_scan_chain mid_inst/ez_reg[1] b_reg[3]
insert_reg_into_scan_chain mid_inst/ez_reg[0] mid_inst/ez_reg[1]
insert_reg_into_scan_chain mid_inst/ez_reg[2] mid_inst/ez_reg[0]
```

Note that insert_reg_into_scan_chain defines a sequential operation, and it must be declared rear member first (b_reg3) before proceeding to the front member (ez_reg2). The resulted sequence is (as shown on Figure 5)

xxx/Q → ez_reg2 → ez_reg0 → ez_reg1 → b_reg3 → yyy/SI

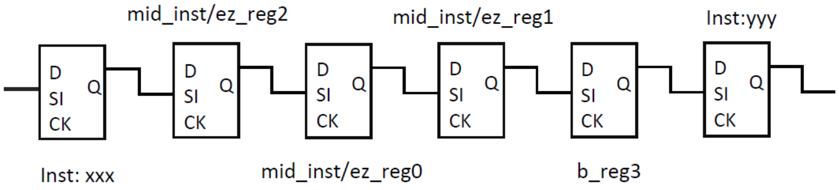


Figure 5: Example of manual scan chain stitching

(4) Removing DFF(s) That Are Connected into Scan Chain

Users can comply with their own DFT design rules more flexibly by manually removing SDFFs that have already been stitched into the scan chain.

Users can specify how to keep or remove a specific register in the scan chain. This usage is a suitable solution for these scenarios:

a. Timing issue, or
b. P&R congestion issue, or
c. User-defined special scan chain function, or
d. Clock generating circuit.

The following command can prevent specific DFF(s) from being stitched into the original scan chain:

```
exclude_add_sdff mid_inst/ez_reg[1]
```

Conversely, the following command prevents specific registers from being removed:

```
exclude_remove_sdff redundant_occ/shift_reg
```

Summary

With ScanChainECO automated flow, modifying scan chain in a functional ECO task is made simple. The benefits of DFT features include:

- By automatically stitching and balancing scan chains, designers no longer need to manually trace the characteristics of each individual SDFF, even when working with large quantities.
- Diverse controllability options provide flexible solutions for achieving DFT-related design requirements.
- Performing logic ECO and fixing scan chains together in one single EasylogicECO flow greatly reduces functional ECO turnaround time.

About the author

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Since joining Easy-Logic Technology in 2021, Kager has been instrumental in leading his team to offer top-notch technical support to users globally. Kager has 18 years of experience in the CAD industry and has worked for companies such as SiS, MStar, MTK, and Cadence. Kager is proficient in the ASIC front-end tool flow, especially in formal verification and ECO applications. Kager also participated in the development of many advanced ECO tool features.