*The Easy Way to Achieve ECO Success*

# EasylogicECO

**Automatic RTL-Based ECO Design Flow Optimized for The Smallest Patch Size**

**EasylogicECO Datasheet**
**DS-ECO-01**

EasylogicECO utilizes an innovative functional ECO algorithm to efficiently complete ECO tasks and reduce the patch size. It makes minimal modifications to the original gate-level netlist based on user's RTL changes, creating a revised netlist that aligns with the updated RTL function.

## Solution Benefits

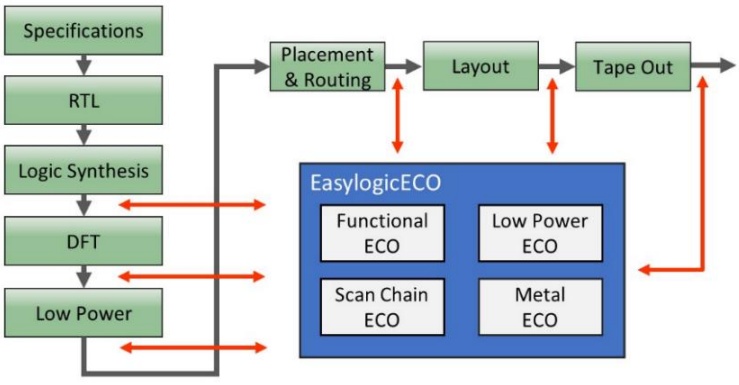
- RTL-based functional ECO solution to preserve the ASIC design flow
- Generating the smallest ECO patch to ensure timing convergence and reduce post-mask costs
- Short ramp-up time for ECO designs of all sizes and complexities
- Scan chain fixing and physical-aware post-layout ECO added for a comprehensive functional ECO flow

## Introduction to Functional ECO (Engineering Change Order)

Functional ECO is an incremental design method commonly used to revise existing ASIC designs. Once RTL code is revised to change the ASIC function, the ECO process modifies a small portion of the existing netlist to align with the revised ASIC function while carefully preserving the integrity of the netlist.

Functional ECO requests have become increasingly frequent in recent years due to the rising complexity of ASIC design and shorter project cycles. As re-spinning the entire design often causes project delays, a successful ECO task offers a shortcut for incorporating the required changes swiftly, upholding time-to-market targets while maintaining the same quality results and the integrity of design flow.

A functional ECO task often needs to address four design aspects: functional logic, scan chain, low power design, and post-layout changes. The ECO solution must also address the same aspects.




EasylogicECO Integration within the ASIC Design Flow

## EasylogicECO Features

**Breakthrough Algorithms for the Smallest ECO Patch**
Leverage the patented GTECH-based equivalence checking algorithm to accurately identify ECO impacts and optimize ECO results, ensuring efficient outcomes.

**Managing Extensive Impact ECOs**
Trace ECO impacts across design hierarchy to identify all required changes within a single run. Support large-scale ECO changes resulting from instantiation of the same ECO block in multiple environments.

**Design-For-Test (DFT) ECO Support**
Automatic SDFF selection and insertion into the scan chain netlist, perform scan chain stitching and length balancing. Support advanced design requirements such as low power design and hold time corrections.

**Support for Advanced Design Requirements**
Consider the impact of design changes in clock domains and voltages domains and apply the needed adjustments automatically, ensuring adherence to user's original design rules while implementing ECO circuit.

**Multiple Spare Resources for Post-Layout ECO Tasks**
Resource options include designated spare cells, filler cells, gate arrays, and disengaged logic cells. Utilize physical information and wire delays to refine logic paths and improve the success rate of the ECO task.

**End-to-End Plug-and-Play Solution for Flow Integrity**
An add-on solution designed to work with the user's existing ASIC flow, complementing flow investments and supporting ECO requests at any design stage.

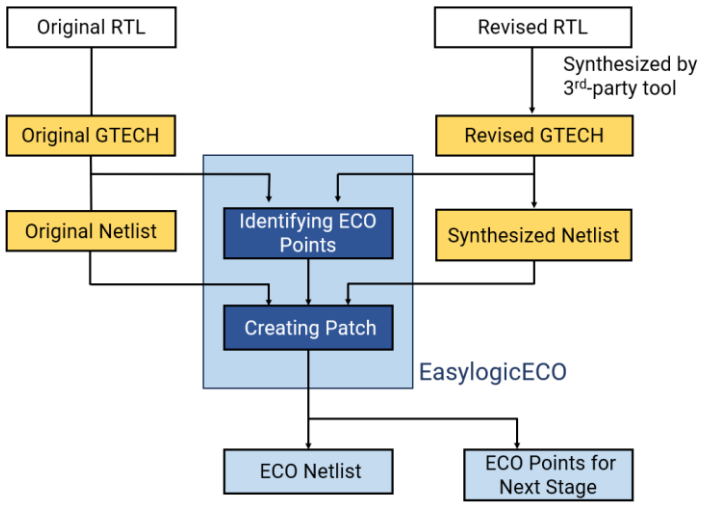
**TCL Script Templates for Easy Ramp-Up**
Script-based operations offer a simple, easy-to-learn user experience, providing seamless integration with mainstream ASIC design flows and support for various process nodes.

## EasylogicECO Design Flow

EasylogicECO seamlessly integrates with the user's existing ASIC design tools, creating a complementary design flow. Starting with an accurate analysis of RTL behavior changes, the EasylogicECO design process maintains the integrity of RTL flow, avoiding the user's making direct modifications on gate-level netlist.

Four simple steps in the EasylogicECO flow:

1. User's making RTL modifications
2. Generating the mapped GTECH netlist using user's synthesis tool
3. Generating the reference gate-level netlist by synthesizing the Revised RTL
4. Creating the ECO netlist, including the original netlist and the ECO patch, and design constraints for the operations downstream




## Technical Support

For more information, please visit https://www.easylogiceda.com/en or email info@easylogiceda.com.