The Easy Way to Achieve ECO Success

EasylogicECO

RTL-Based Automatic Functional ECO Solution Optimized for The Smallest Patch Size

EasylogicECO Datasheet
DS-ECO-01

A successful functional engineering change order (ECO) operation swiftly implements the required RTL revisions during the late stages of design, upholding time-to-market goals without compromising design quality or integrity.

EasylogicECO's advanced algorithm minimizes patch sizes, making precise adjustments to the original gate-level netlist to align it perfectly with the updated RTL functionality.

Solution Benefits

- RTL-based ECO solution to preserve the ASIC design flow
- Generating the smallest ECO patch to ensure timing convergence and reduce post-mask costs
- Short turnaround time for ECO designs of all sizes and complexities
- Scan chain fixing added for a comprehensive functional ECO flow

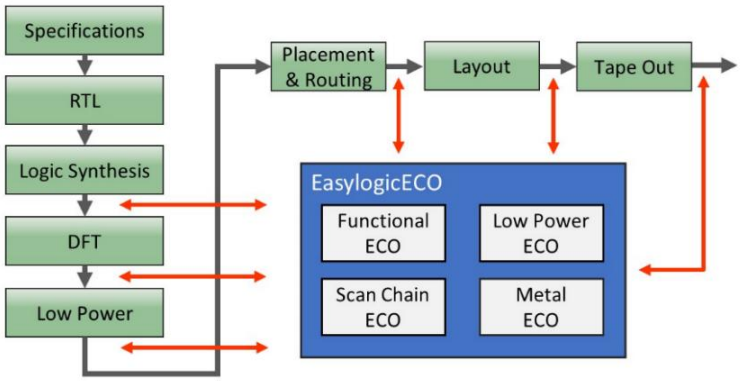
Scope of Functional ECO Operation

Functional ECO operations typically address four design areas: functional logic changes, scan chains, low-power design, and metal-only post-layout implementation.

The success of a functional logic change lies in accurately identifying design differences at the RTL level and generating the smallest possible logic patch. Metal-only ECO requires achieving timing closure while implementing logic changes using available spare resources. Scan chain and low-power adjustments are required only when the relavent logic is modified; however, tracking these logic changes can be challenging for designers.

A functional ECO operation can occur at any stage of the ASIC design cycle. It must adapt to the user's complex and often heterogeneous tool environment, accurately capture design data, generate a design rule-compliant patch, and deliver precise instructions for result verification.

It is crucial to fully understand the design's performance goals at each step before initiating an ECO operation. Designers should clearly define the requirements to ensure the ECO outcomes generated align perfectly with these objectives.



EasylogicECO Integration within the ASIC Design Flow

EasylogicECO Features

Breakthrough Algorithms for the Smallest ECO Patch
Leverage the patented GTECH-based equivalence checking algorithm to accurately identify ECO impacts and optimize ECO results, ensuring efficient outcomes.

Managing Extensive Impact ECOs
Trace ECO impacts across design hierarchy to identify all required changes within a single run. Support large-scale ECO changes resulting from instantiation of the same ECO block in multiple environments.

Design-For-Test (DFT) ECO Support
Automatic SDFF selection and insertion into the scan chain netlist, perform scan chain stitching and length balancing. Support advanced design requirements such as low power design and hold time corrections.

Support for User's Specific Design Requirements
Allow users to enter design rules and constraints, including clock and voltage domains, and apply the needed ECO adjustments automatically, ensuring adherence to user's original design requirements while implementing ECO logic.

Multiple Spare Resources for Post-Layout ECO Tasks
Resource options include designated spare cells, filler cells, gate arrays, and disengaged logic cells. Utilize physical information and wire delays to refine logic paths and improve the quality of routing changes.

Plug-and-Play for Easy Flow Integration
An add-on solution designed to work with the user's existing ASIC flow, supporting ECO requests at any design stage and complementing tool investments.

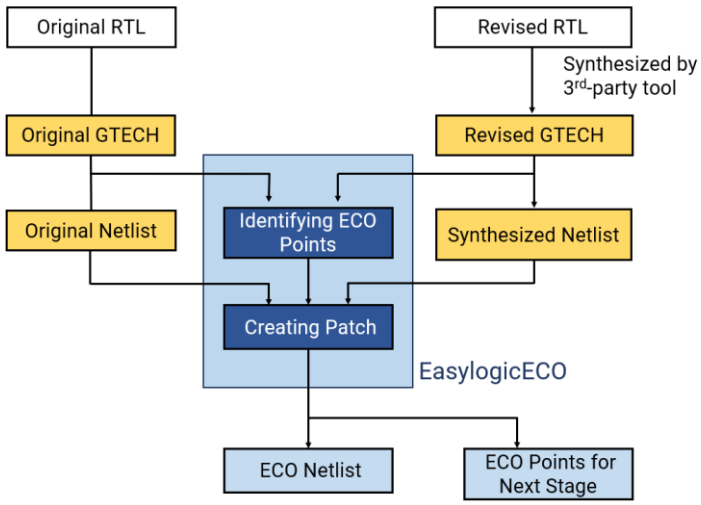
TCL Script Templates for Rapid User Ramp-Up
Script-based operations offer a simple, user-friendly experience, closely integrating with the design constraints of the existing ASIC to provide a comprehensive understanding of the ECO goals.

EasylogicECO Design Flow

Starting with an accurate analysis of functional changes, the EasylogicECO design process maintains the integrity of RTL flow, avoiding the user's making direct modifications on gate-level netlist.

Four simple steps in the EasylogicECO flow:

1. User makes RTL modifications
2. Generate the mapped GTECH netlist using the user's synthesis tool
3. Generate the reference gate-level netlist by synthesizing the Revised RTL
4. Create the ECO results, including the revised netlist, ECO logs, and design constraints for the downstream operations



Technical Support

For more information, please visit https://www.easylogiceda.com/en or email info@easylogiceda.com.